

## CONCLUSION

In the present Amendment, the Specification and claims 1, 9, and 17 have been amended; claims 21 and 22 have been added. Therefore, pending claims 1-22 are presented for consideration by the Examiner. If the Examiner has any questions, comments, or suggestions, the undersigned earnestly requests a telephone conference.

Respectfully submitted,



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## ATTACHMENT A

“Marked-up” amendments as follows:

### In the Specification:

Page 4, line 25, after the phrase “when forming” please delete “an” and substitute therefor --a--.

Page 5, line 26, after the phrase “wide interconnect needs” please insert --to--.

Page 13, lines 23-24, after the phrase “from 0.5 micron to 50 micron” please delete the following text: **[Gentlemen, are the dimensions and spacings listed here for the trenches correct?]**.

### In the Claims:

1. (Amended) A method [for providing a substantially planar semiconductor topography which extends above a plurality of electrically conductive features that form an integrated circuit], comprising:

etching a plurality of laterally spaced dummy trenches into a dielectric layer between a relatively wide trench and a series of relatively narrow trenches;

filling said [dummy trenches and said wide and narrow] trenches with a conductive material;

polishing said conductive material to form dummy conductors [exclusively] in said dummy trenches and interconnect [exclusively] in said narrow and wide trenches, wherein said dummy conductors are electrically separate from [said plurality of] electrically conductive features [and co-planar with said interconnect] of an ensuing integrated circuit.

9. (Amended) A method [for providing a semiconductor topography having a plurality of electrically conductive features and a topography which is substantially planar], comprising:

etching a plurality of laterally spaced dummy trenches into a dielectric layer between a trench which is to receive a relatively wide interconnect feature and a series of trenches which are to receive [a] relatively narrow interconnect [feature] features;

filling said plurality of dummy trenches with a conductive material; and

polishing said conductive material to form dummy conductors [bounded exclusively within], wherein said dummy [trenches] conductors are electrically separate from [said] electrically conductive features[, and such that first upper surfaces of said dummy conductors are substantially co-planar with second upper surfaces of said relatively wide and narrow interconnect features] of an ensuing integrated circuit.

17. (Amended) A substantially planar semiconductor topography [elevationally raised above a plurality of electrically conductive features which receive electrically transitory voltages forwarded through an integrated circuit], comprising:

a plurality of laterally spaced dummy trenches [residing within] in a dielectric layer, between a relatively wide trench and a series of relatively narrow trenches;

dummy conductors [bounded exclusively within] in said dummy trenches and electrically separate from [said plurality of] electrically conductive features below said dummy conductors; and

[interconnect bounded exclusively within] conductive lines in said narrow and wide trenches, wherein [interconnect] upper surfaces of said conductive lines are substantially coplanar with dummy conductor upper surfaces.

21. (Added) The method of claim 1, wherein said dummy conductors are substantially coplanar with said interconnect.

22. (Added) The method of claim 9, wherein said dummy conductors are substantially coplanar with said interconnect.